Dynamic Electric Model for IGBT Power module based on Q3D® and Simplorer® : 3D Layout Design, Stray Inductance Estimation, Experimental Verifications

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Abstract— **The layout of power modules is one of the key points in power module design, especially for high power densities, where couplings are increased**. **Stray inductances cause various problems in switching devices and should be minimized at an early design stage to avoid later required countermeasures and redesign after the device prototype has been built. In this paper**, **using Ansys® Q3D® Extractor, electromagnetic simulation is carried out to extract and evaluate the inductive and resistive parasitics of one phase of a three-phase automotive inverter module with rating of 650 V – 400 A. The purpose is to develop and verify the electrical model including parasitic parameters for the studied phase-leg operating as a chopper.**

The switching behavior of the studied structure is analyzed based on Ansys® Simplorer® simulation, and a dynamic electrical model is carried out. Experimental test measurements are performed. The comparison between the simulation models and the experimental data is reported and conclusions are made.

Keywords—3D modelization; stray inductance; Ansys® Q3D®; Simplorer®; electric dynamic model; double pulse.

I. INTRODUCTION

One of the major concerns of designing the package layout of a power module is the parasitic inductances within the module. When the power switch is turning off, the energy stored in the stray inductance of a commutation loop and a high di/dt of the switching component will cause voltage spikes and ringing with the parasitic capacitances of the device. Voltage spikes are a common reason of the switching component failure. Thus, a poorly designed layout might result in severe turn-off overvoltage and electromagnetic interference and compatibility (EMI/EMC) problems that will strongly affect the safe operation of the module. With the new demands of lower loss, lower cost and smaller size, numerous soft switching technics have been developed for higher switching frequency; power switches can then operate faster and faster, which makes EMI problems even more critical [1]. To keep stray inductance low is a basic requirement in package design of insulated-gate bipolar transistor (IGBT) modules. Thus, how to deal with the parasitics effect will ultimately affect the EMI, efficiency, and performance of a converter [2].

Various concepts could be then developed to decrease the stray inductance of the commutation loops of power modules. Here, we describe some eventual prospects of this article [3];

- Reduce the size of the control and power loops, by integrating the gate drivers and (part of) the DC bus capacitance directly on the same substrate as the power devices,
- Integrate some common-mode filtering directly in the power module, as close as possible to the source of common-mode current.

In this paper, the knowledge of the switching component internal structure is used to estimate the parasitic parameters of a phase-leg commutation loops. The parasitic parameters such as resistor, self-inductance and mutual inductance of the layout are extracted by Ansys® Q3D® Extractor. A 3D model of a phase-leg of a three phase-leg inverter module with all dimensions is modeled in Ansys® Design Modeler®. The modelling of the parasitic parameters of the commutation loops with a detailed electrical model of the studied phase-leg is presented.

II. SIX-PACK ALL-SI INFINEON POWER INVERTER MODULE

Power module manufacturers have developed dedicated products to meet automotive requirements. To make the study more coherent with the industry standard package, a commercial 650 V – 400 A IGBT module was selected. The HybridPACK™ 1 FS400R07A1E3 manufactured by Infineon is an automotive qualified power inverter designed Hybrid Electric Vehicle (HEV) applications for a power range up to 20–30kW. The HP1-SixPACK Inverter modules consist of twelve IGBT switches each with anti-parallel diode. Fig. 1(a) shows the picture of the power inverter considered in this article. The module size is 140 mm×72 mm×17mm.

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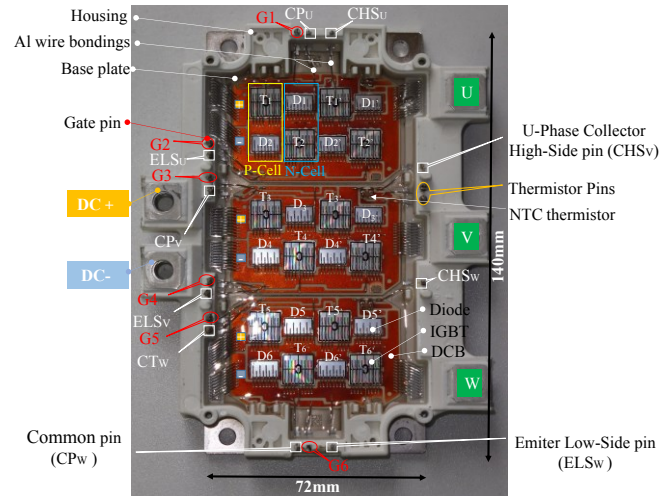
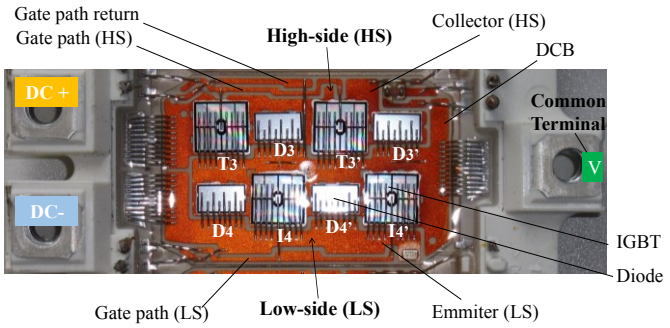
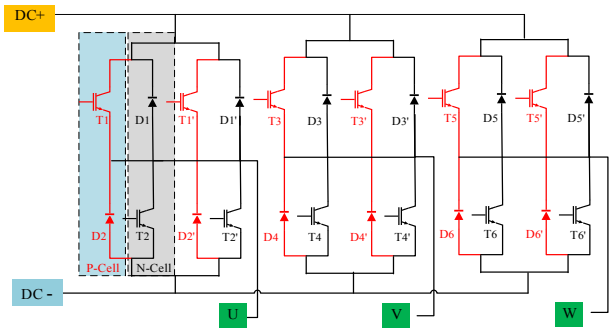


(a)



(b)



(c)

Fig. 1. Structure of six-pack FS400R07A1E3 power module. (a) Module picture. (b) Phase leg picture (c). Circuit diagram.

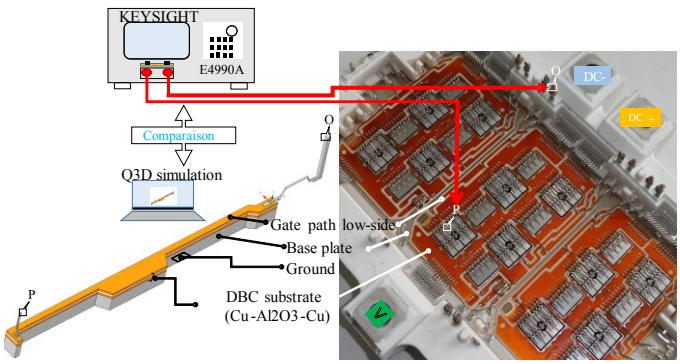
To form the complete three-phase inverter, three identical DBC 38.5 mm×38.5 mm substrates are bonded to a copper base plate and connected in parallel by connecting the substrates to common DC+ and DC- terminals. The module has five power terminals (DC+, DC-; U, V, and W).

To monitor the collector-emitter voltages Vce and control the gate-source voltages Vgs, Au over Ni-plated brass pins are bonded to the metal traces on the direct bond copper substrates, so the module has six control terminals for the gate circuit (G1 to G6), three Collector High-Side Pins (CHS_U, CHS_V and CHS_W), three Emitter Low-Side Pins (ELS_U, ELS_V and ELS_W) and three common terminal pins (CP_U, CP_V and CP_W). An NTC resistor for temperature sensing is integrated in the module. The upper arm of each phase contains two IGBT chips and two free-wheeling diodes. The lower arm is structured in the same way.

Fig. 1(b) shows the phase-leg picture, each switching element is composed of two paralleled 9.73 mm × 10.23 mm 650 V normally-off Si IGBTs (e.g. T_3 and $T_{3'}$) with two antiparallel 9.2 mm× 5.44mm 650 V fast switching Si diodes (e.g. D_3 and $D_{3'}$). As can be seen in Fig. 1(c), each phase-leg of studied module is constructed based on two parallel P-cell and N-cell concept. This packaging method reduces the parasitic inductance in the commutation loop, suppresses the LCR resonance, which consists of parasitic inductance in the module and the capacitance in the power devices, during switch turn-on and turn-off. The system performance and reliability can be then improved [4].

III. Stray Inductance Estimation and Experimental Verification

Q3D® performs electromagnetic field simulation using a combination of the FEM and the Method of Moments (MoM). This tool performs a DC and an AC analysis and avoids the meshing of the air. The results provided by this software consider proximity and skin effects. For the inductance estimation the information about geometry and materials is required. The current directions are specified by assigning the sources and sinks [5]. Thus, before the entire parasitic elements of the studied V-phase-leg were imported to a circuit simulator, in the bellow section, a comparative analysis of Q3D® calculation results (Fig. 2(a)) and measurement of an impedance analyzer is made. A case study of the substrate layout design of the FS400R07A1E3 gate path low-side of the phase-leg V is given. Experimental tests have been done to extract its stray inductance (Fig. 2(b)).



(a) (b)

Fig. 2. Q3D evaluating results. (a) Q3D simulation. (b) Inductance and resistance measurement setup.

The measurement was performed using the KEYSIGHT E4990A impedance analyzer, which has frequency range from 20 Hz to 30 MHz.

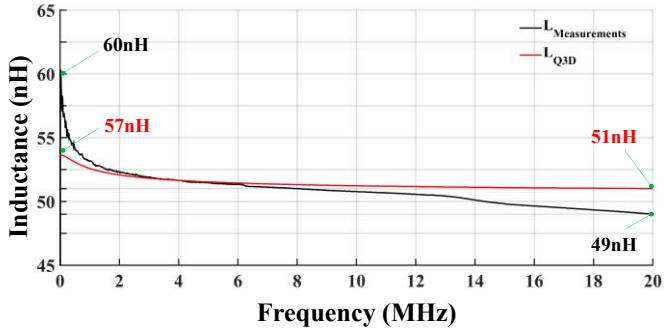


Fig. 3. Comparison between Q3D inductance calculation and measurements.

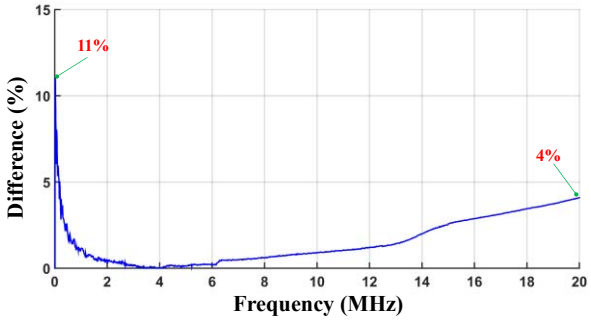


Fig. 4. Difference between Q3D parasitic inductance estimation and measurements.

The measurement setup is shown in Fig. 2(b). The sweeping frequency was set from 20 Hz to 20 MHz. In order to measure the parasitic inductance, the E4990A pin probes from the impedance analyzer were connected to P and O, as shown in Fig. 2. After the calibration of the impedance analyzer and probes, a set of inductance curves was obtained. Fig. 3 is the inductance curve between terminal P and O. The black curve is the measured curve ($L_{Measurements}$). The red curve is from Q3D simulation (L_{Q3D}). Fig. 4 is the error between Q3D simulation and measurement. According to these curves, L_{Q3D} curve is close to $L_{Measurements}$ curve with only 11% maximum error observed.

IV. Parasitcs Extraction: a Case Study

A phase leg power module is a basic configuration unit for a variety of power converters in modern power electronic modules. In this section, a substrate layout design of a phase-leg of the FS400R07A1E3 three-phase power module is studied. The geometry is drawn in Ansys® Design Modeler® (Fig. 5) and then exported to Ansys® Q3D® for the parasitic element extraction. The gate paths are not considered in this study. The detailed dimensions of the studied phase leg are listed in Table I.

Fig. 6 shows the substrate layout of the studied phase-leg. Under inductive loads, the commutating devices are upper arm (IGBT T_3 and IGBT $T_{3'}$) and lower arm (diode D_4 and $D_{4'}$), or upper arm (diode D_3 and $D_{3'}$) and lower arm (IGBT T_4 and $T_{4'}$). From now, we consider that when load current I_{load} is flowing out of the output terminal of the V-phase, current commutates between the upper arm IGBTs T_3 and IGBT $T_{3'}$ and lower arm diodes D_4 and diode $D_{4'}$. The conducting paths before and after commutation are shown in Fig .6

TABLE I. Physical Size and Materials of the Phase-Leg

Power section DBC Size (mm)	35 × 54		
DBC thikness (mm)	0.28(Cu) 0.31(Al_2O_3)		
Base-plate dimensions(mm)	72 ×140		
Base-plate thikness(mm)	2 (Cu)		
IGBT Size(mm)	9.73 × 10.23		
Diode size(mm)	9.2 × 5.44		
DC bus and Output terminal Wire Bonding	Length (mm)	11.9	(Al)
	Diameter (μm)	200	
Diode Wire bonding	Length (mm)	4.61	(Al)
	Diameter (μm)	200	
IGBT Wire bonding	Length (mm)	7.3	(Al)
	Diameter (μm)	200	

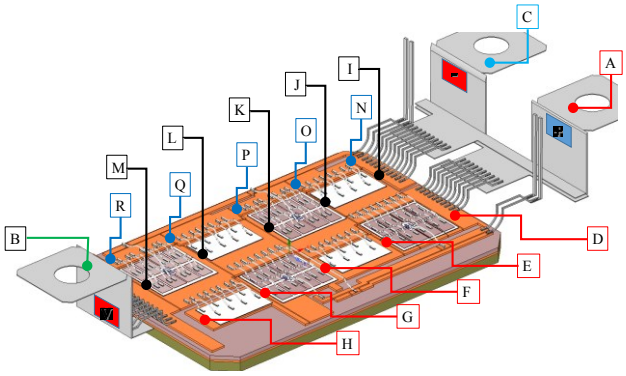


Fig. 5. 3-Dimension view of the V-phase leg of HP1 FS400R07A1E3 power module layouts with measuring points.

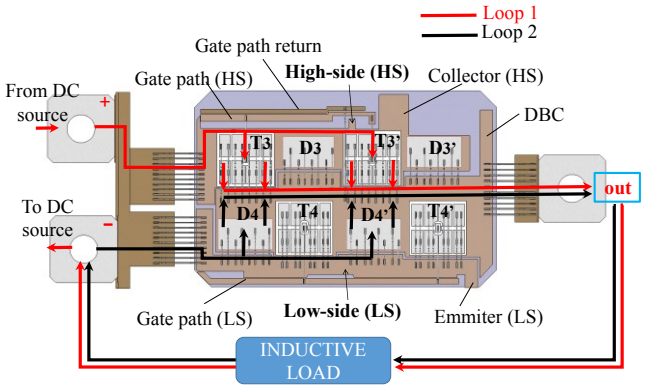


Fig. 6. Power section layout of the the V-phase leg of HP1 FS400R07A1E3.

Fig 7 shows the equivalent circuit of the V-phase-leg of FS400R07A1E3 power module including L-R parasitics. To obtain accurate parasitic parameters, we divide the layout include copper on the substrate and wire bonding into several

sections. Then, we get matrix contains resistors and self-inductance shown in Fig. 7.

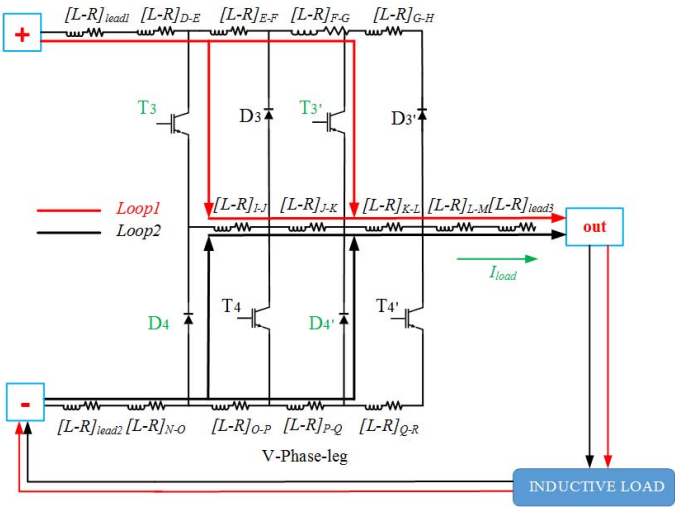


Fig. 7. Equivalent circuit of the V-phase leg of HP1 FS400R07A1E3.

TABLE II. SELF-INDUCTANCE AND RESISTANCE FOR EQUIVALENT CIRCUIT SHOWN IN FIG. 7

Name	L(nH)	R(μΩ)	Name	L(nH)	R(μΩ)
[L-R]lead1	9.8	200.24	[L-R]J-K	1.8	48.6
[L-R]lead2	8.5	169.7	[L-R]K-L	1.9	55.3
[L-R]lead3	5.3	112.2	[L-R]L-M	2	44.4
[L-R]D-E	1.8	68	[L-R]N-O	2.7	137.7
[L-R]E-F	2.19	73.4	[L-R]O-P	2.9	157.8
[L-R]F-G	2	64.1	[L-R]P-Q	3	140.35
[L-R]G-H	2.5	78.6	[L-R]Q-R	3.4	179
[L-R]I-J	1.7	55.6			

Since the resistance does not affect transient behavior much, while it affects the steady state current distribution, the resistance is extracted under the condition of DC excitation. Otherwise the partial stray inductance are extracted under AC excitation [6]. The stray capacitances of the ceramic insulator are not considered in this study.

Assuming that the studied phase-leg operates as a chopper under inductive load, parasitic elements of the commutations loops are identified under Q3D® as follows:

The sources and sinks, which are the measuring points, are shown in Fig. 5. The path from A to D is the positive bus bar, the path from C to I is the negative bus, and the path from B to M is the AC output bus bar. There are two conduction paths: through T3–T3' which is loop1 shown in Fig. 6 and Fig. 7, and through D4–D4' which is loop2.Thus, when calculating loop1, the materials of T3 and T3' are set to copper and the materials of D3, D3', T4, T4', D4 and D4' are set to silicon, implying that only the T3–T3' path conducts. The other path is calculated in the same way. $[L\text{-}R]_{lead1}$, $[L\text{-}R]_{lead2}$, $[L\text{-}R]_{lead3}$ are stray inductances and parasitic resistances of the positive, negative and output terminals respectively. $[L\text{-}R]_{D\text{-}E}$, $[L\text{-}R]_{E\text{-}F}$,$[L\text{-}R]_{F\text{-}G}$, $[L\text{-}R]_{G\text{-}H}$, $[L\text{-}R]_{I\text{-}J}$, $[L\text{-}R]_{J\text{-}K}$, $[L\text{-}R]_{K\text{-}L}$, $[L\text{-}R]_{L\text{-}M}$, $[L\text{-}R]_{N\text{-}O}$, $[L\text{-}R]_{O\text{-}P}$, $[L\text{-}R]_{P\text{-}Q}$, $[L\text{-}R]_{Q\text{-}R}$ are the L-R parasitic parameters on the substrate including wire bonds and DBC copper traces.

Table II shows the value of R-L parasitic parameters. These values come from the L-R matrix extracted by Q3D® analysis at 15 kHz operating frequency. From Table II, we can find that DC and common terminals connections make up the dominant parasitic inductance inside the packaging of commutation loop. This is due to the long wire bonding connections in these terminals. The stray inductance of the commutation loop1 is 22.8nH extracted by Q3D®. The stray inductance of the commutation loop2 is 22.6nH. We can find also that the contribution of the DC bus and output terminal to the total stray inductance in each commutation loop is above 60% in these conditions.

V. SIMULATIONS

The purpose of this section is to develop an electrical model including parasitic parameters for the studied structure. The simulation models in this study are made for IGBT/Diode component of HP1FS400 power module. Then, the models are completed with R-L parasitic parameters extracted previously with Q3D®. The same component is characterized in experimental tests as well.

The simulation software used in this article is Simplorer 15 from Ansys®. The software offers three different IGBT models in its characterizing wizard; Averaged IGBT, Basic Dynamic IGBT, and Advanced Dynamic IGBT [7]. The Advanced Dynamic model is selected in this work because it includes the modelling of a tail current in IGBT turn-off and the effects of different input capacitances as well. Free-wheeling diodes are also modeled separately. Dynamic behavior of each diode is included and taken in account.

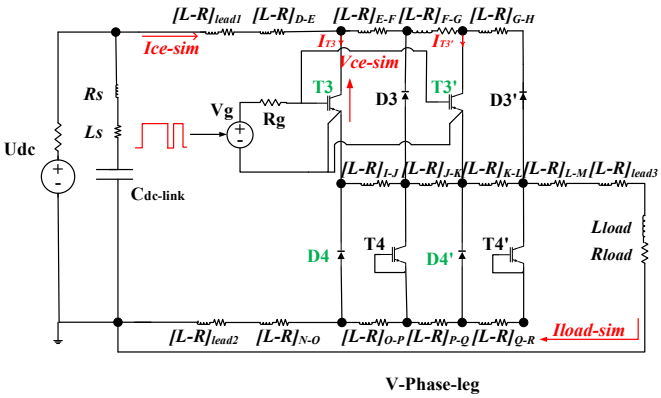


Fig. 8. Simplorer simulation circuit of the studied phase leg.

A simple circuit diagram of the simulation model is presented in Fig. 8. Vce_sim is the simulated voltage of the upper arm, Ice_sim is the simulated current of IGBT T3 and IGBT T3'. The gate circuit is modelled only with an external gate resistor Rg and with a controlled voltage source Vg. The IGBT circuit feeds and R-L load in a chopper mode. The parasitic elements (Ls, Rs) of the DC-link capacitor come from an impedance measurements. The simulation parameters for the circuit elements are presented in Table III. From the research project point of view the most interesting quantities are the amplitude

of the voltage spike at IGBT turn-offs and amplitude of current spikes at IGBTs turn-ons.

TABLE III. MODEL AND TEST SETUP PARAMETERS

Parameter	Value	Parameter	Value
Lload	124µH	Udc	170
Rload	24mΩ	Cdc-link	300 µF ±10%
Rg	5Ω	Ls	25 nH
Vg	±15V	Rs	1 mΩ

VI. DYNAMIC TESTS

To experimentally verify the accuracy of the developed electrical model of the studied phase-leg completed with L-R parasitic elements, dynamic tests are done on the studied structure. The circuit diagram of the test system is shown in Fig. 9. Chopper circuit and double pulse test method are adopted. The test equipment used are listed in Table IV.

TABLE IV. TEST EQUIPMENT

Oscilloscope	**Type :** LECROY WaveSurfer 10 **Sample rate :** 10 GS/s **Bandwidth :** 1GHz
Diferrential Voltage Probe	**Type :** TLEDYNE LECROY HVD3106 **Bandwith :** 120MHz **Input impedance :** 10M Ω, 5pF **Accuracy :** 1%
Coaxial Shunt	**Type :** SDN-414-025 **Bandwidth :** 1200MHz **Resistance :** 0.025Ω **Maximum energy :** 3J
DC Source	**Type :** TDK-Lambda **Power :** 2400 W **Voltage :** 600 V **Current :** 4 A

During the test, lower arm (IGBT T_4 and IGBT $T_{4'}$) is kept off, and a double pulse drive signal is put on the upper IGBTs (T_3 and $T_{3'}$) simultaneously. As shown in Fig. 9, Vce_exp is the measured voltage of the upper arm, Ice_exp is the measured current of IGBT T_3 and IGBT $T_{3'}$ tested with the coaxial shunt. The test points of Vce are collector high side pin (point ①) and common terminal pin (point ②) as shown in Fig. 9. During the measurements, the load is connected between point ③ and point ④. Ice collector current is measured from coaxial shunt at point ⑤.

The double-pulse tester is traditionally used for testing IGBTs in dynamic commutation situations. In this test setup, both IGBT turn-off and turn-on events are recorded during one measurement sequence. The typical waveforms of double pulse tester used in this work is represented in Fig. 10.

The first pulse (48µs) will be used to charge the load inductor to the testing current. (i.e. 60 A in our case), and then the switch is turned off. As a result, current commutates to the diode and turn off characteristic could be captured. After a short while (16µs), a shorter pulse (16.2µs) is applied and the device is turned on. Due to the existence of the large inductive load, the current (I_{load}) does not change much, and the turn on characteristic will be obtained at desired current. Both measurements and simulation are conducted under 170 V, 60A.

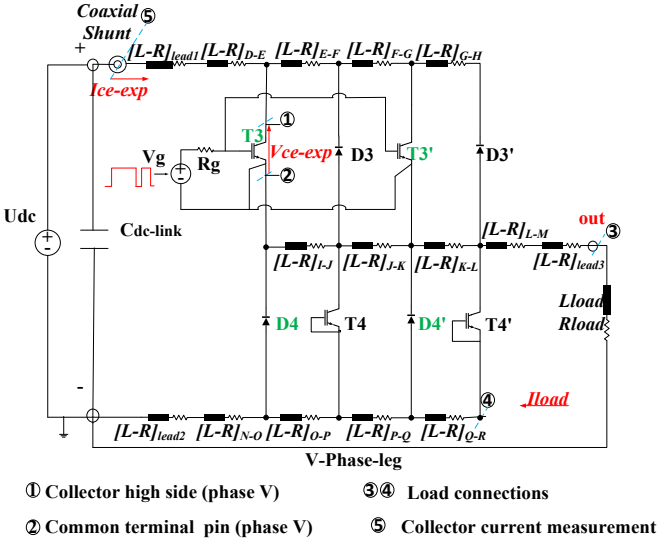


Fig. 9. Circuit diagram of test system.

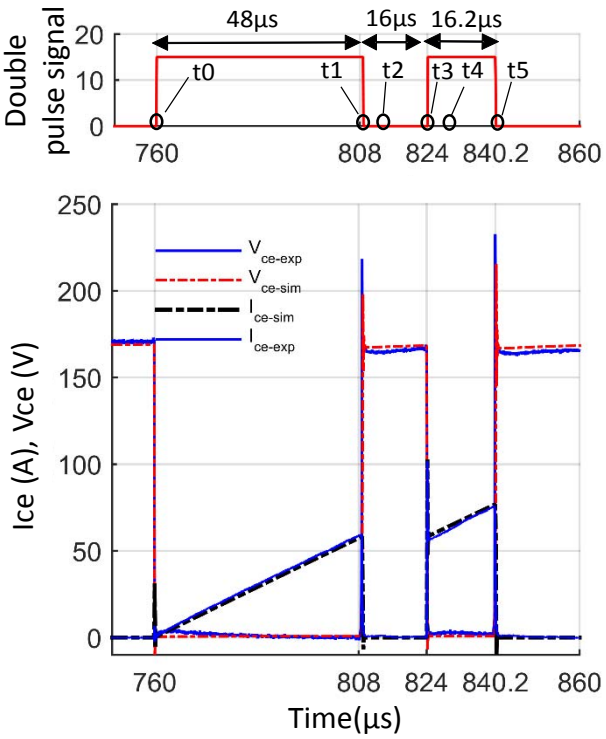


Fig. 10. Typical waveforms of double pulse test.

VII. Results and Discussion

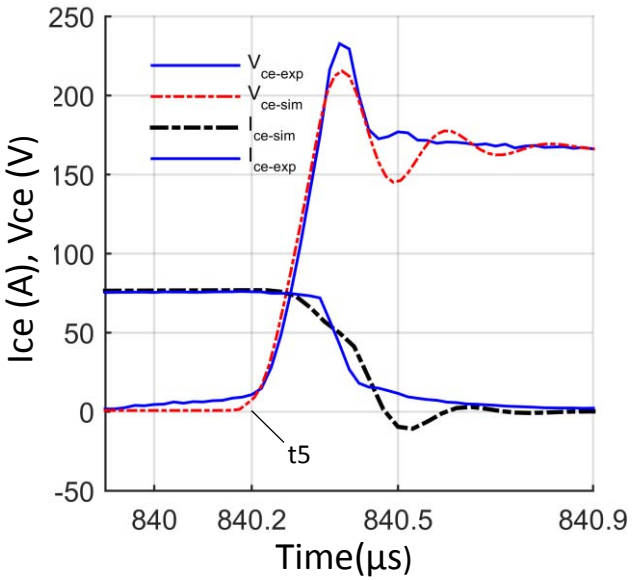


Fig. 11. IGBT Turn-off Comparison between Simulation and Measurements

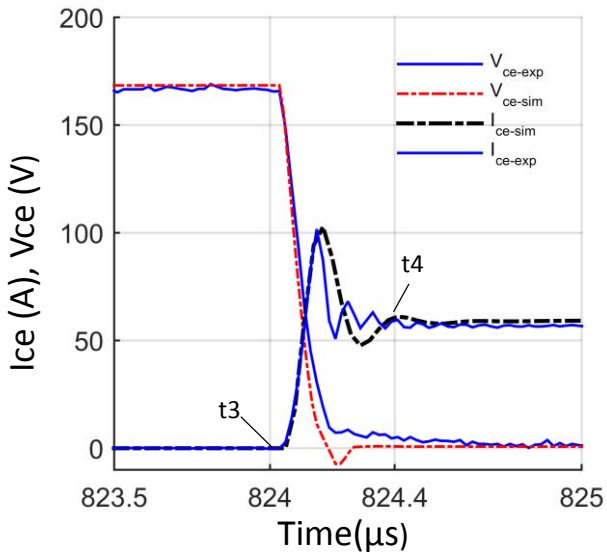


Fig. 12. IGBT Turn-on Comparison between Simulation and Measurements

It can be seen from Fig. 11 and Fig. 12 that the static and dynamic behavior of developed electrical model completed with R-L parasitics are globally in accordance with the measurement.

The voltage across the IGBT during turn off is shown in Fig. 11. The simulated Vce ($V_{ce\text{-}sim}$) oscillates at the turn-off duration. The oscillation during turn-on and turn-off process is triggered by not only the stray inductance but also the device capacitance in the IGBT and diode [6]. Thus, the calculated stray inductance introduced by the package and the capacitance of the modeled IGBTs/Diodes compose a resonant circuit that causes voltage and current oscillation at switching [6]. The voltage spike in the simulation is not exactly the same as in the hardware measurement; the voltage overshoot is 220V in the simulation, while the overshoot voltage is 240 V in the measurement. Forward recovery voltage of the diode is not taken into account in this study, it might contribute to the total voltage overshoot.

Fig. 12 displays the IGBT turn-on Vce and Ice curves for both simulation and measurements. It can be seen that the current and voltage behavior of the model at turn-on is acceptable comparing with the measurement.

Comparing these curves, we can see that the agreement between the simulation and measurements are generally acceptable. However, the oscillation frequency of simulated Ice_sim is not the same as the measured oscillation frequency of Ice_exp. Hence, the limitation of the Simplorer IGBT/Diode models could be a reason that causes some mismatches between simulation results and measurements. In addition the parasitic capacitance, load, DC link capacitor and cables have to be modeled to probably enhance the dynamic behavior of the model.

VIII. Conclusion

In this study, the estimation of the stray inductance of a phase-leg commutation loops is considered. A detailed model of the structure is created and used to verifying the Q3D® inductance estimation and switching devices models of Simplorer®. From the above discussions and experiments, some conclusion can be drawn:

Q3D® inductance calculation is verified by measurement. This extraction tool can be used to find out the correct parasitic inductance parameter.

The static and dynamic behavior of the developed electrical model completed with L-R parasitics is globally satisfactory and achieve an acceptable accuracy. Nevertheless, the dynamic behavior of the model, typically the oscillation frequency at switching on or off, can be improved to match the oscillation frequency of the tested device.

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